REMARKS

Applicants thank the Examiner for the through consideration given the present application. Claim 1-14 are pending in this application. Claims 1, 5, 10, 12 and 14 are independent and are amended. Reconsideration of this application, as amended, is respectfully requested.

Rejection Under 35 U.S.C. § 102(b) and 103(a)/Allowable Subject Matter:

Claims 1-3 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,684,555 to Shiba et al. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiba et al. in view of U.S. Patent No. 5,945,984 to Kuwashiro. Claim 14 is rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,995,189 to Zhang in view of U.S. Patent No. 6,400,438 to Noritake et al. These rejections are respectfully traversed.

Claims 5, 7, 8 and 10-13 are objected to as being dependent upon a rejection base, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6 and 9 are allowed. Applicants thank the Examiner for the indication of allowable subject matter. Claims 5, 10 and 12 are rewritten in independent form including all of the limitations of base and any intervening claims, and are therefore allowable over the applied prior art of record.

While not conceding the appropriateness of the rejections, but merely to advance prosecution of the instant application, independent claim 1 is amended to recite a combination of elements in a liquid crystal device,

including a "source PCB and the gate PCB being formed along a first side and a second side, respectively, of the lower substrate and outside the area in which the sealant is formed such that the upper substrate is not formed over the source PCB or the gate PCB, wherein the first and second sides meet at a corner of the lower substrate," and "a plurality of transmitting wires on the lower substrate, the transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB in the vicinity of the corner of the lower substrate."

Independent claim 14 is amended to recite a combination of steps in a method of fabricating a liquid crystal display device, including "forming a sealant on the first substrate, wherein the gate transmitting wires connect the gate pads to the source pads across the sealant in the vicinity of a corner of the first substrate."

It is respectfully submitted that the combinations of elements and method steps set forth in independent claims 1 and 14 are not anticipated or made obvious over the applied prior art of record, including Shiba et al., Zhang, Noritake et al., or Kuwashiro.

In contrast to Applicants' claimed invention, Shiba et al. discloses a liquid crystal display panel, including an array substrate 200 and a counter substrate 500 arranged to face each other and adhered to each other with a sealing agent 113 in a sealing region 111, as shown in Fig. 1. Data lines X are connected to data line pads 761 to 764 and scanning lines Y are connected to scanning line pads. A first wiring line 127 is guided along a second shorter

side 201d to a second longer side 201b and connected to power supply pads 735 to 738. The first wiring line 127 is divided into five narrow lines, serving as second wiring lines 123-4, which are guided across the seal region 111 and connected to output leads of wiring film 718 via a common pad, as shown in Fig. 3. Shiba et al. does not teach or suggest a source PCB and a gate PCB being formed along a first side and a second side, respectively, of the lower substrate and outside the area in which the sealant is formed, such that the upper substrate is not formed over the source PCB or the gate PCB, wherein the first and second sides meet at a corner of the lower substrate and a plurality of transmitting wires being electrically connected with the gate and source pads across the sealant such that the source PCB is electrically connected with the gate PCB in the vicinity of the corner of the lower substrate, as recited in claim 1.

In rejecting claim 4, the Office Action relies on Kuwashiro for teaching of disposing dummy pads between data pads to inspect and repair a display. However, Kuwashiro does not teach or suggest the above cited limitations of claim 1 incorporated in claim 4, and therefore fails to cure the deficiencies of Shiba et al. with respect to claim 1.

With respect to the rejection of claim 14, Zhang shows a pixel section 202 formed on a substrate 201, signal line drive circuit 203, and scanning line drive circuit 204, as well as signal lines 205, formed on the pixel region 202, gate insulating film 206 formed on each of the components 203, 204, 205 and gate electrodes 207, 208, 209 formed on the gate insulation film 206, as shown in Fig. 2a. Zhang et al. does not teach or suggest forming a sealant on a first

substrate, wherein the gate transmitting wires connect the gate pads to the source pads across the sealant in the vicinity of a corner of the first substrate.

The Office Action relies on Noritake et al. for teaching of insulator substrates which are cut away by scribing and breaking of a mother class board. However, Noritake et al. does not teach or suggest the above cited limitations of claim 14 and therefore fails to cure the deficiencies of Zhang as a primary reference.

In view of the foregoing, it is respectfully submitted that independent claims 1, 5, 10, 12 and 14 patentably distinguish over the cited art, take alone or in combination, and reconsideration and withdrawal of the rejections under 35 U.S.C. §§ 102(b) and 103(a) are respectfully requested. Since the remaining claims depend directly or indirectly from allowable independent claims, they should also be allowable for at least the reasons set forth above, as well as the additional limitations provided by these claims. Therefore, all pending claims should be in condition for allowance.

As the Examiner will note, also enclosed herewith are thirteen (13) sheets of corrected formal drawings, wherein the margins of said drawings have been adjusted as requested in the PTO-948 form. Entry thereof is respectfully requested.

CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

If there are any outstanding issues, however, the Examiner is invited to telephone Sam Bhattacharya, Reg. No. 48,107, at (703) 205-8000 in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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Attachments: thirteen (13) drawings